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PRE-APPEAL BRIEF REQUEST FOR REVIEW	Docket Number (Optional) 7090 P2 107262.202US1

	Application Number	Filed
	10/623666-Conf. #5063	July 21, 2003
	First Named Inventor: Claes BJORKMAN et al.	
	Art Unit: 2874	Examiner: S. U. Song

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant /inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☐ attorney or agent of record. Registration number _____
- ☒ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. 32,590

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March 15, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of 1 forms are submitted.

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as First Class Mail, in an envelope addressed to: MS AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: March 15, 2006 Signature: _____ (Eric L. Prahl)

The examiner rejected claims 1-10 under 35 U.S.C. §103(a) as being unpatentable over Delwala (U.S. 6,658,173) in view of Johnson et al. (U.S. Publication 2002/0181825), Nakamura (U.S. 6,449411), and Fitzgerald (U.S. 6,680,495).

In rejecting the claims, the Examiner characterizes Delwala as teaching a second semiconductor layer that is laterally divided into two regions; and as support of this assertion she points to Fig. 1. But a close reading of the description that accompanies Fig. 1 does not support the Examiner. Delwala does not disclose a second semiconductor layer that is laterally divided into two regions, as required by claim 1.

Delwala's Fig. 1, to which the Examiner directs our attention, is a "logical diagram" of an integrated optical/electronic circuit. It does not show how the chip is physically divided into different regions but rather it shows how the devices that are fabricated on Delwala's chip are grouped into three different logical groupings. Delwala's description of Fig. 1 makes this clear, as do Delwala's comments describing Fig. 1. According to Delwala, "FIG. 1 shows a logical diagram of an integrated optical/electronic circuit" and:

> While the pure optical functions 10, the pure electronic functions 12, and the opto-electronic functions 14 are illustrated at distinct locations on the wafer 152, in actuality the devices that perform these functions are each typically physically interspersed across the wafer 152. [emphasis added] (Col. 10, lines 42-47+)

The Examiner acknowledges, that "Delwala does not expressly disclose said optical signal distribution circuit to be designed to provide signals to the microelectronic circuit to be fabricated in the first region of the second semiconductor layer at said later time." And the Examiner also admits that:

> Delwala also does not expressly disclose the first region into which fabrication of the microelectronic circuitry has not yet begun. As noted above, Delwala discloses the first regions comprising the microelectronic circuitry (i.e., fabrication already begun). *It is noted that the method of forming the device is not germane to the issue of patentability of the device itself.* [emphasis added]

To address these admitted deficiencies in Delwala, the Examiner relies on the other two references, namely, Johnson and Fitzgerald.

Before dealing with these other two references, we first note that Delwala is fundamentally at odds with the claimed invention. Or, stated differently, **Delwala teaches away from creating the claimed structure**. This is because one of Delwala's objectives is to fabricate both his microelectronic circuitry and his optical devices at the same time and by using

the same fabrication processes. Indeed, Delwala goes to great lengths to select optical component designs that enable him to do precisely that.

In his Background, Delwala identifies one of his goals as follows:

> It would be desirable to provide active optical waveguide device functionality and/or passive optical waveguide device functionality based largely on the CMOS devices and technology as well as manufacturing methods that allow for simultaneous fabrication of optically active and passive waveguide elements. [emphasis added] (Col. 1, lines 62-67).

And Delwala selects device designs that enable him to achieve this objective. This is made clear at various places in the Delwala specification including the following:

> ... the devices that can perform the pure optical functions 10, the pure electronic functions 12, and the opto-electronics functions 14 can be produced concurrently, on the same wafer 152, and using the same manufacturing process.
>
> The passive optical waveguide devices 800, the electronic devices 5101, and the active optical waveguide devices 150 can each be fabricated using standard CMOS processing techniques and technology. In one embodiment, the passive optical waveguide devices 800, the electronic devices 5101, and the active optical waveguide devices 150 are described as being fabricated on a single Silicon-on-Insulator (SOI) wafer 152. For example, pure electronic devices such as field effect transistors (FETs) can be deposited and/or etched on the SOI wafer 152. The passive optical waveguide devices 800 and the active optical waveguide devices 150 can be simultaneously deposited and/or etched on the SOI wafer 152. The masks, and the positioning equipment, that are used for etching active optical waveguide devices 5101 can also be used to etch the passive optical waveguide devices 800 and the active optical waveguide devices 150 as described herein. [emphasis added] (Col. 10, line 62 to col. 11, line 20).

And again, towards the end of the specification, Delwala notes that:

> VLSI and CMOS masks are used to simultaneously deposit and/or etch on a single SOI wafer 152 one or more passive optical waveguide devices 800, one or more active optical waveguide devices 150, and/or one or more electronic devices 5101. [emphasis added] (Col. 44, lines 11-19).

In other words, Delwala avoids pursuing a fabrication process in which he would produce a structure having the optical circuitry but none of the microelectronic circuitry that is also intended to be part of the structure.

In summary, Delwala sets as his objective, fabricating the optical circuitry and the microelectronic circuitry concurrently using the same CMOS fabrication techniques. As a consequence of that, at no point during the fabrication of a circuit according to Delwala would you ever have a structure of the type recited in the claims.

The Johnson Patent

We also note that Johnson does not supply that which is missing from Delwala. Moreover, Delwala and Johnson actually teach away from the combination that is proposed by the Examiner.

Johnson forms his optical components using materials (e.g. III-V semiconductor compounds). Devices formed by such materials would be damaged by the high temperatures required by typical microelectronic fabrications processes. This is explicitly pointed out in paragraphs [0001], [0167] and [0168], the last one of which is quoted below:

> [0168] Component processing in materials such as monocrystalline silicon is typically carried out at temperatures above about 800° C., while component processing in compound semiconductor materials such as GaAs is typically carried out at lower temperatures, between about 300° C. and about 800° C., and components formed in GaAs would be damaged by the higher temperatures of silicon processing (although the unprocessed GaAs itself would not be damaged). Therefore, preferably components such as component 4256 are formed first in silicon substrate 4201 using high-temperature processing. Components such as component 4268 are then formed in the GaAs island 4204 at the lower processing temperatures, which will not damage the already formed silicon components 4256. [emphasis added]

This means that Johnson deliberately fabricates his optical structures after the microelectronic circuitry has been fabricated. Johnson avoids fabricating his optical devices earlier in his fabrication process because those optical devices would be destroyed by the heat used to fabricate the microelectronic circuitry.

Moreover, the two references (Delwala and Johnson) have opposing objectives. As pointed out, the objective of Delwala is to fabricate the optical structures concurrently with the fabrication of his microelectronic circuitry; whereas the objective of Johnson is to fabricate them after the fabrication of his microelectronic circuitry. Not only do they teach away from the combination proposed by the Examiner, neither of them teaches a process that would at any stage of the fabrication process yield the structure of claim 1. That is, at no stage of either fabrication process would there be a structure that includes two laterally arranged regions of the same layer wherein one region contained optical signal distribution circuitry and the other region was of a quality sufficient to receive microelectronic circuitry that was not yet fabricated into that region.

The Fitzgerald Patent

The examiner also admits that Delwala "does not expressly disclose the first region into which fabrication of microelectronic circuitry has not yet begun." So, the Examiner relies on Fitzgerald to supply this missing aspect. The Examiner argues:

> ...a method of forming an article of manufacture comprising an optical ready substrate made of a first semiconductor layer 308, an insulating layer 310, and a second semiconductor layer 306 or 312, wherein the second semiconductor layer is laterally divided into two regions including a first region and a second region, the first region into which fabrication of microelectronic has not yet begum (see Figures 6a and 6b) and being of quality that is sufficient to permit microelectronics circuitry to be fabricated therein at a later time (as evidenced by the fabrication of the COS circuitry shown in Figure 6c).

The Examiner points to Figs. 6a and 6b of Fitzgerald and argues that: substrate 308 corresponds to the first semiconductor layer of claim 1; SiO_2 layer 310 corresponds to the insulating layer of claim 1; and either Si cap layer 306 or Si cap layer 312 corresponds to the second semiconductor layer of claim 1. But if that is true, then Fitzgerald does not in fact supply that which is missing from the other two references.

We note that in the structure shown in Figs. 6A-C, the layers which the Examiner identifies as corresponding to the second semiconductor layer of claim 1 (i.e., layers 306 and 312) along with the underlying oxide layer 310 are completely etched away in the regions in which the microelectronic circuitry is to be formed so as to expose the underlying "pristine substrate" (see Fig. 6B) that lies beneath the oxide layer 310. According to Fitzgerald:

> In one embodiment as illustrated in FIGS. 6A-6C, a starting wafer heterostructure 600 based on the resulting structure shown in FIG. 3D, Si CMOS electronics 602 can be processed on the Si substrate. In this embodiment, an early step would include patterning the wafer to define the optoelectronic receiver areas, and these areas would be protected with a mask. The other areas would be etched down to the Si substrate, leaving a virgin Si surface to be processed into CMOS electronics. (Col. 6, lines 28-36).

It is into this exposed "pristine substrate" that the CMOS circuitry is fabricated.

In contrast, claim 1 requires that the first and second regions be laterally arranged portions of the second semiconductor layer. But if Si cap layer 306 (or Si cap layer 312) corresponds to the second semiconductor layer, as argued by the Examiner, then that cap layer is the layer that should receive the microelectronic circuitry. But according to Fitzgerald, before the microelectronic circuitry is fabricated, this cap layer is completely removed and the microelectronic circuitry is fabricated in substrate 308, which according to the Examiner corresponds to the first semiconductor layer of claim 1. That is, in the Fitzgerald structure, the

microelectronic circuitry is fabricated into the first semiconductor layer (which incidentally is below the insulating layer), not into the second semiconductor layer, as required by the claims. So even if Fitzgerald was combined with Delwala and Johnson, that combination would not yield the claimed invention.

In the Advisory Action, the Examiner put forward another analysis of Fitzgerald, noting that "Fitzgerald additionally discloses an embodiment wherein the microelectronic circuitry is formed in the Si cap layer rather than the Si substrate (column 4, lines 28-64)." But in that other embodiment, Fitzgerald explicitly inserts an insulating layer 400 between top Si cap layer 402 and optically active layer 404 to isolate optically-active layer 404 from the CMOC electronics fabricated in Si cap layer 402. So, even in that embodiment, the microelectronic circuitry and the optical signal distribution circuit are not formed in the same layer, as required by the claims.